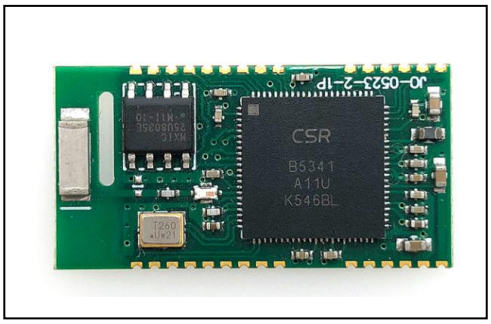
JS&T 金瓯科技



Customize service and solution for wireless transportation products

Bluetooth Module Hardware Datasheet

BTM0612C2P

Chongqing JINOU Science and Technology Development Co., Ltd.

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Contents

1. Features

■Bluetooth® v4.1 specification compliant

■Radio includes integrated balun and typical RF performance of 7 dBm transmit power and -90 dBm receive sensitivity (π/4-DQPSK modulation)

■ 80 MHz RISC MCU

■ 8 Mb internal ROM

■ Programmable DSP with 4K x 32-bit program RAM and 12K x 24-bit for data RAM

■ 6 programmable digital I/Os

■ 2 analogue I/Os

■ Serial interfaces: UART, USB 2.0 full-speed, I℃, SPI

■ 4 on dedicated LED interface

■ Wide Supply-Voltage Range

VBAT Pin Nominal Supply Voltage at 2 .65V ~ 4.2 V

USB_VBUS Pin Nominal Supply Voltage at 3.6V ~ 6.5V

■ Module Size:28×14.5 （unit：mm error = ±0.2mm）

2. Product Description

The CSR5341 Module is CSR's next generation IC for wireless HCI and wireless HID applications.
The CSR5341 Module is a radio and baseband IC for Bluetooth 2.4 GHz systems, which integrates most of the functionality required by gaming devices into a single IC. It minimises the number of external ICs and components required.

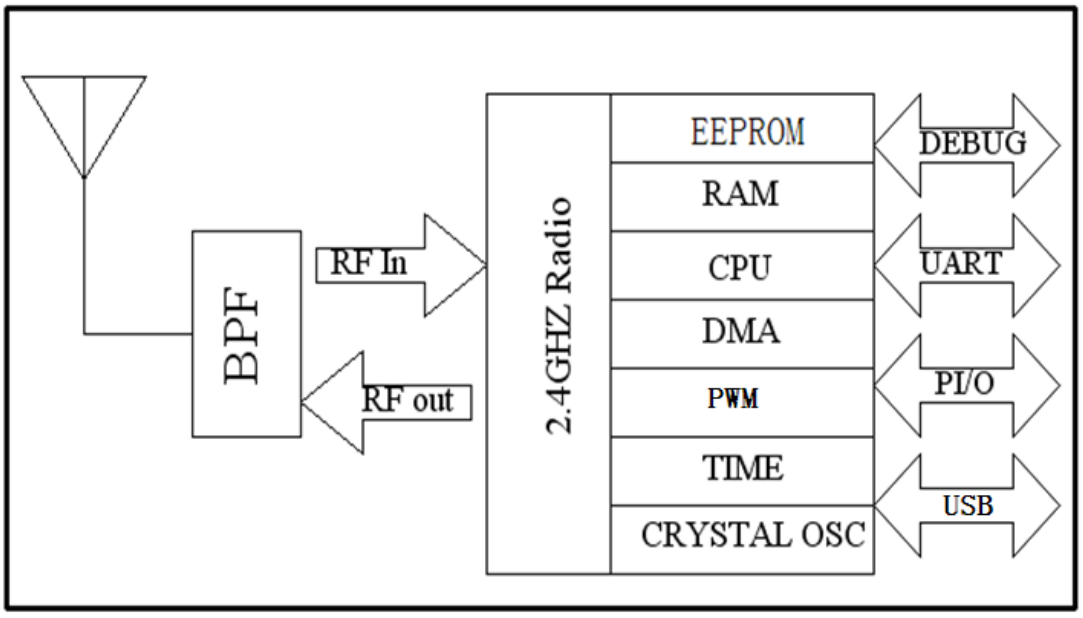
The CSR5341 Module integrates an application processor with internal ROM, a power management subsystem and LED drivers in an SoC IC.

The CSR5341 Module contains a large number of programmable and analogue I/Os, which are required for interfacing to various sensors, e.g. keyboards, button pads, gyros and accelerometers.

3. Applications

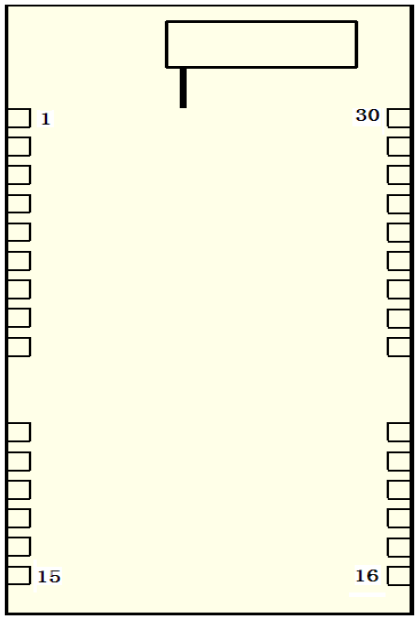
Wireless gaming controllers
Wireless HID
Wireless HCI

4. Block Diagram



5. Pin Descriptions

5.1 Device Terminal

No.	Description		Description	No.
1	AIO0		GND	30
2	AIO1		GND	29
3	RESET		VDD-LDO	28
4	SPI-MISO		LED0	27
5	SPI-CSB		LED1	26
6	SPI-CLK		LED2	25
7	SPI-MOSI		LED3	24
8	UART_CTS		USB-DM	23
9	UART_RTS		USB-DP	22
10	ART_TX		PIO12	21
11	UART_RX		PIO13	20
12	VREG		PIO14	19
13	VBAT		PIO28	18
14	GND		PIO29	17
15	USB_VBUS		PIO30	16

5.2 Device Terminal Functions

PIN	NAME	DESCRIPTION
1	AIO0	Analogue programmable I/O line.

2	AIO1	Analogue programmable I/O line.
3	RESET	Reset input, active-low
4	SPI-MISO	SPI data output
5	SPI-CSB	Chip select for SPI, active-low
6	SPI-CLK	SPI clock
7	SPI-MOSI	SPI data input
8	UART_CTS	UART clear to send active low or PIO5
9	UART_RTS	UART request to send active low or PIO4
10	UART_TX	UART data output
11	UART_RX	UART data input
12	VREG	Connect Key to Vbat
13	VBAT	Connect to battery positive terminal
14	GND	Connect to GND
15	USB_VBUS	Connect to USB_VBUS line of USB interface
16	PIO30	programmable I/O line. or I℃ WP line
17	PIO29	programmable I/O line. or I℃ data line
18	PIO28	programmable I/O line. or I℃ clock line
19	PIO14	programmable I/O line.
20	PIO13	programmable I/O line.
21	PIO12	programmable I/O line.
22	USB-DP	Usb data plus with selectable internal 1.5K pull-up resistor
23	USB-DM	Usb data minus
24	LED3	Connect to LED
25	LED2	Connect to LED
26	LED1	Connect to LED
27	LED0	Connect to LED
28	VDD-LDO	Do Not Connect This Pin
29	GND	Connect to GND
30	GND	Connect to GND

6. Electrical Specifications

6.1 ABSOLUTE MAXIMUM RATINGS

rating	MIN	MAX	UNIT
USB (USB_VBUS) operation	-0.4	6.5	V
Battery (VBAT) operation	-0.4	4.4	V
LED[0:3] voltage	-0.4	4.4	V
Storage temperature range	–40	85	℃
Other terminal voltages	Vss-0.4	Vdd+0.4	V

6.2 RECOMMENDED OPERATING CONDITIONS

rating	MIN	TYP	MAX	UNIT

Operating temperature range	-20	20	70	℃
USB (USB_VBUS) operation	3.6	5	6.5	V
Battery (VBAT) operation	2.65	3.3	4.2	V
LED[0:3] voltage	1.1	3.2	4.3	V

6.3 Input/Output Terminal Characteristics

Digital Terminals [PIO]

input voltage	MIN	TYP	MAX	UNIT
VIL input logic level low	-0.4		0.25xVDD	V
VIH input logic level high	0.7 x VDD		VDD +0.4	V
Tr/Tf			25	ns
output voltage				
VOL output logic level low, lOL = drive strength specified in table			0.4	V
VOH output logic level high, lOH = drive strength specified in table	0.75xVDD			V
Tr/Tf			5	ns

Input and tristate currents	MIN	TYP	MAX	UNIT
With strong pull-up	-150	-40	-10	uA
With strong pull-down	10	40	150	uA
With weak pull-up	-5	-1	-0.33	uA
With weak pull-down	0.33	1	5	uA
CI input capacitance	1		5	pF
High impedance state (no pulls)	-0.1	0	0.1	uA

AIO

Input /Output voltage level	MIN	TYP	MAX	UNIT
Input logic level low	-0.4	-	0.25xVDD_AIO	V
Input logic level high	0.7 xVDD_AIO	-	VDD_AIO +0.4	V
Output logic level low	-	-	0.4	V
Output logic level high	0.75xVDD_AIO	-	-	

LED Driver pads

Input /Output voltage level		MIN	TYP	MAX	UNIT
Current Ipad	High impedance state			5	uA
	Current sink state			50	mA
LED pad	Vpad<0.5V	2.4	2.8	4.4	ohm

resistance					

6.6 ESD Protection

Apply ESD static handling precautions during manufacturing. Table shows the ESD handling maximum ratings.

condition	class	Max rating
Human Body Model Contact Discharge per JEDEC EIA/JESD22-A114	2	2000V (all pins)
Charged Device Model Contact Discharge per JEDEC EIA/JESD22-C101	III	300V (all pins)

7. CIRCUIT DESCRIPTION

Memory Management Unit

The MMU provides dynamically allocated ring buffers that hold the data that is in transit between the host, the air or the Kalimba DSP. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers. The use of DMA ports also helps with efficient transfer of data to other peripherals.

System RAM

56 KB of integrated RAM supports the RISC MCU and is shared between the ring buffers for holding voice/data for each active connection and the general-purpose memory required by the Bluetooth stack.

Kalimba DSP RAM

Additional integrated RAM provides support for the Kalimba DSP:

- 4K x 24-bit for data memory 1 (DM1)
- 8K x 24-bit for data memory 2 (DM2)
- 4K x 32-bit for program memory (PM)

Note:

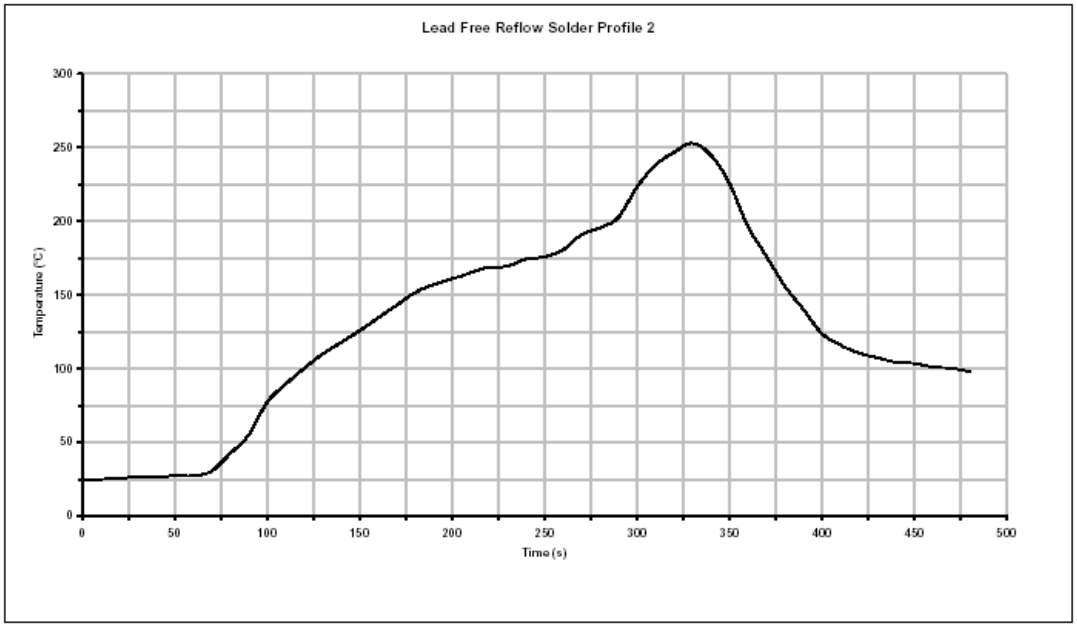
The Kalimba DSP can also execute directly from internal ROM or external SQIF, using a 1K-instruction on-chip
cache.

Internal ROM

8 Mb internal ROM contains system firmware.
Production Information Page 30 of 66 Confidential Information -This Material is Subject to CSR's Non-disclosure Agreement CS-316607-DSP6 © Cambridge Silicon Radio Limited 2014-2015 www.csr.com

8. Solder Profiles

Composition of the solder ball: Sn 95.5%, Ag 4.0%, Cu 0.5%



Typical Lead-Free Re-flow Solder Profile

Key features of the profile:

- Initial Ramp = 1-2.5 ℃/sec to 175 ℃±25 ℃ equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250 ℃) = 3 ℃/sec max.
- Time above liquidus temperature (217 ℃): 45-90 seconds
- Device absolute maximum reflow temperature: 260 ℃

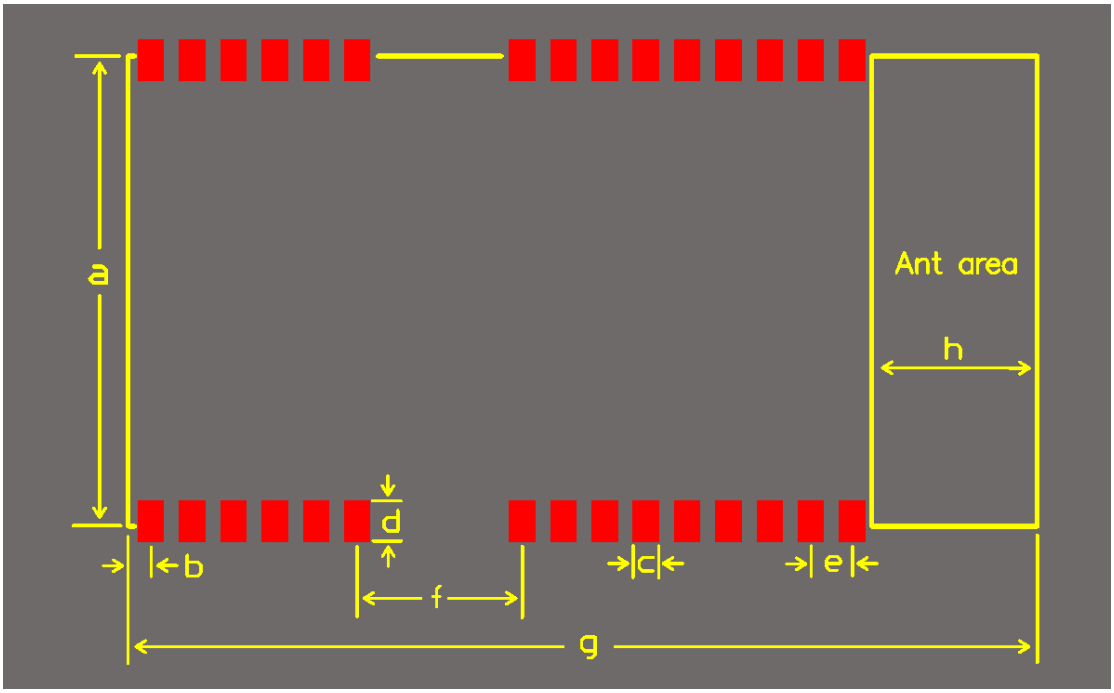
Devices will withstand the specified profile. Lead-free devices will withstand up to three reflows to a maximum temperature of 260 ℃.

Notes：They need to be baked prior to mounting。

9. Physical Dimensions

Recommend PCB Layout

a	b	c	d	e	f	g	h	Unit
570	27.874	32	50	50	200	1102.4	200	mil
14.5	0.708	0.813	1.27	1.27	5.08	28	5.08	mm


a
Ant area
h
d
b
f
c
e
g